IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#12 / Reply Brief 11-29-03

Applicant:	STEVEN C. DAKE; PAUL E. LUSE	Group Art Unit:	2782
Serial No.:	09/469,277	Examiner:	Dwin M. Craig
Filed:	December 22, 1999		
For:	METHOD FOR MODELING HARDWARE USING SOFTWARE	Atty. Dkt. No.:	INTL-0278-US (P7627)

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Sir:

Applicants respectfully file this Reply Brief in response to the Examiner's Answer mailed on August 26, 2003.

I. REPLY

The Answer asserts that Savitzsky discloses defining a plurality of hardware devices as a plurality of objects. In this regard, the Examiner asserts that FIG. 2 of Savitzsky shows hardware devices 200 and 210 being defined as a plurality of software objects 160. Examiner's Answer, p. 27. However, Savitzsky instead discloses that element 160 is merely "general programming-system functions". Savitzsky, 5:36. Thus Savitzsky does not disclose defining a plurality of hardware devices as a plurality of software objects, and the rejection of claims 1 and 2 should be reversed.

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11-14-2003

Date of Deposit: October 14, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Jennifer Juarez

With regard to claims 6-10, the Examiner erroneously contends that Muller discloses a redundant array of independent disks modeled by a plurality of objects. Answer, pp. 29-30. In this regard, the Examiner contends that I/O nodes 212 are used to model the redundant array of independent disks as a plurality of objects. However, Muller discloses that the I/O nodes 212 are merely nodes to connect a computing node 200 with various disks 224. Muller, 4:57-64. Thus the I/O nodes 212 do not "abstract the array's of redundant disks," as contended by the Examiner. Answer, p. 30. More so, Muller does not disclose modeling the redundant array of independent disks by a plurality of objects. Instead, the storage disks 224 are used to store storage resource objects; nowhere does Muller disclose modeling the disks themselves by a plurality of objects. Muller, 17:8-56. Thus claims 6-10 are patentable and the rejection should be reversed.

With regard to the rejection of claims 16-18 over Brumley in view of Morris, the Examiner points to columns 1 and 3 of Morris (Answer, p. 30) to provide the motivation to combine its disclosure with Brumley. However, as noted in columns 1 and 3, Morris is merely directed to a system for configuring a personal computer (i.e., a configurator); in no way does Morris relate to software for modeling operation of a computer, and certainly not to modeling a plurality of disk objects thereof. This is especially so, as FIG. 4 of Morris (further relied on by the Examiner for teaching modeling a plurality of disks as disk objects, Answer, p. 32) merely indicates that one of a number of disks may be selected for incorporation into a configuration of a PC. Nowhere does Morris teach or suggest modeling a plurality of disks as disk objects. *See* Morris, 10:22-35. This is particularly true, as Morris discloses that an end-product computer created using the configurator includes only a single hard disk. Morris, 5:30-40.

With respect to the Examiner's arguments noted in Section D (pp. 32-33 of the Answer), it is respectfully submitted that the Examiner erroneously refers to claims 6-10.

For the same reasons discussed above respecting Savitsky and Muller, claims 28-32 are patentable and the rejection should be reversed.

With regard to the Examiner's arguments regarding enablement of claims 1-17 and 19-21, the Examiner erroneously points to elements not present in the claims. Specifically, the Examiner asserts that the above claims are not enabled because the Specification does not include a UML diagram. Answer, p. 35. Such a diagram however is nowhere set forth in the claims, nor is required by Patent Office or Federal Circuit precedent. E.g., *Fonar Corp. v. General Electric*, 41 U.S.P.Q.2d 1364 (Fed. Cir. 1997). Instead, the application includes a number of block diagrams and a flowchart of operation of one embodiment of the invention. *E.g.*, FIGS. 5-12.

Furthermore, the Examiner's enablement rejections are inconsistent with the Examiner's assertion that many of the same claims are obvious under 35 U.S.C. § 103. In this regard, the Examiner states that "the abstraction of the detail functioning of the different components in a computer system provides a simple method of having those components interact, without a programmer having to understand all of the complexities of the lower level details implementation. The idea of abstracting a software module, using object technology, to reduce the complexity is one of the primary motivations for using software abstraction." Answer, p. 31. It is thus inconsistent for the Examiner to assert claims as not enabled while at the same time asserting that such claims would be obvious to one skilled in the art. For these further reasons, the claims are enabled and the rejection of claims 1-17 and 19-21 should be reversed.

II. CONCLUSION

For the reasons set forth herein, as well as set forth in the Appeal Brief, Applicants respectfully request that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: October 14, 2003

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